CLAIMS

1. Integrated circuit comprising:

a main oscillator circuit supplying a first clock signal;

a peripheral circuit supplying a periodic wake-up signal;

a central processing unit having a first operating mode at full power, in which the first clock signal is applied to the central processing unit; an active halt mode, in which the main oscillator circuit and the central processing unit are deactivated, the central processing unit being awakened by the periodic wake-up signal;

characterized in that it comprises a secondary oscillator circuit for supplying a second clock signal of lower frequency than the first clock signal;

a circuit for managing clock signals arranged for, upon the wake-up of the central processing unit at the end of the active halt mode, waking up the secondary oscillator circuit and applying the second clock signal to the central processing unit so as to clock the central processing unit to the frequency of the second clock signal and thus obtain a second operating mode with reduced current consumption relative to the first operating mode.

2. The integrated circuit according to claim 1 wherein the main oscillator circuit is deactivated during at least one part of the second operating mode to reduce the current consumption.

3. The integrated circuit according to claim 1 wherein the circuit for managing clock signals is arranged for waking up the secondary oscillator circuit and deactivating the main oscillator circuit upon the wake-up of the central processing unit and during the second operating mode.

4. The integrated circuit according to claim 1, comprising means for going from the second operating mode with reduced current consumption to the first operating mode at full power.

5. The integrated circuit according to claim 4 wherein the circuit for managing clock signals is arranged for:

waking up the main oscillator circuit;

deactivating the secondary oscillator circuit;

applying the first clock signal to the central processing unit, so as to go from the second operating mode to the first operating mode.

6. The integrated circuit according to claim 1, comprising means for going from the first operating mode, to the second operating mode, without deactivating the central processing unit.

7. The integrated circuit according to claim 1 wherein the circuit for managing clock signals is arranged for simultaneously waking up the main and secondary oscillator circuits and for applying the second clock signal to the central processing unit so as to have a third operating mode of transition between the first two operating modes during a stabilization time interval.

8. The integrated circuit according to claim 1 wherein the circuit for managing clock signals comprises:

a switch circuit for supplying, either the first clock signal, or the second clock signal, at the clock signal input of the central processing unit; and

a control circuit comprising means for waking up/deactivating the main oscillator circuit, means for waking up/deactivating the secondary oscillator circuit and means for actuating the switch circuit so as to send the first or the second clock signal to the central processing unit.

9. The integrated circuit according to claim 1 wherein the circuit for managing clock signals comprises a clock output and is arranged for having the following switch states:

a first switch state, in which the management circuit supplies the first clock signal at the clock output;

a second switch state, in which the management circuit supplies the second clock signal at the clock output; and

a transient state between the first state and the second state, in which the management circuit does not supply any clock signal at its clock output, the clock output being set to a determined electric level, so as to avoid interference upon the switch transition between the two clock signals.

10. The integrated circuit according to claim 1 wherein the circuit for managing clock signals is arranged so that a halt command of the central processing unit interrupts the operating mode in progress and triggers the active halt mode, in which the main and secondary oscillator circuits are deactivated and no clock signal is sent.

11. The integrated circuit according to claim 1 wherein the circuit for managing clock signals is arranged for performing a reconfiguration operation, when a halt command is applied while the first clock signal is being applied to the central processing unit, an operation in which the secondary oscillator circuit is awakened and the second clock signal is pre-selected to be applied to the central processing unit, so as to automatically wake itself up in the second operating mode with reduced current consumption at the end of the halt mode.

12. The integrated circuit according to claim 1 wherein the circuit for managing clock signals is arranged for deactivating the main and secondary oscillator circuits, if and only if a halt command is applied.

13. The integrated circuit according to claim 1 wherein the circuit for managing clock signals is controlled by a control register of the central processing unit comprising:

a first flag for waking up the main oscillator circuit;

a second flag for waking up the secondary oscillator circuit; and

a third flag for selecting the transmission of the first or of the second clock signal.

14. The integrated circuit according to claim 13 wherein the control register further comprises a flag controlled by a counter of stabilization cycles that is active during the third operating mode.

15. The integrated circuit according to claim 1 wherein the secondary oscillator circuit has reduced current consumption relative to the main oscillator circuit.

16. The integrated circuit according to claim 1 wherein the secondary oscillator circuit has a negligible stabilization time relative to the main oscillator circuit.

17. The integrated circuit according to claim 1 wherein the secondary oscillator circuit is of resistance capacitance type.

18. A circuit comprising:

a central processing unit;

a plurality of clock circuits, each of the clock circuits having a different clock speed and consuming different amounts of power;

a clock management circuit coupled to the central processing unit and to the plurality of clock circuits, the clock management circuit being constructed to receive a plurality of clock signals and to output one of the clock signals to the central processing unit;

a wakeup circuit having a clock wakeup circuit therein, the clock wakeup circuit providing an output which is coupled to both the management circuit and to the CPU for providing a signal to the CPU through a connection other than through the clock management circuit and providing a signal to the clock management circuit.

19. The circuit according to claim 18, further including:

an interrupt decode circuit coupled between the clock wakeup circuit and the CPU for providing a signal from the clock wakeup circuit to the CPU.

20. The circuit according to claim 18 wherein a first clock within the plurality of clocks is a high speed clock for operating the CPU at approximately its highest rated speed; and a second clock of the plurality of clocks being a low speed clock circuit, operating at a substantially slower frequency than the first clock circuit and operating itself and the CPU in a low power mode.

21. The circuit according to claim 20 wherein said second clock circuit reaches a stabilization in fewer cycles of its own clock than the first clock signal reaches a stabilization cycle within cycles of its own clock.

22. A method of operating a circuit comprising:

operating a CPU at a first high frequency provided by a high frequency clock;

halting the operation of the CPU and placing it in a sleep mode;

halting the operation of the high frequency clock for at least a part of the time while the CPU is in sleep mode so that during this time period both the CPU and the high frequency clock are in sleep mode;

awakening the CPU under control of the wakeup clock after the CPU has been in sleep mode for a period of time;

inputting a low frequency clock to the CPU upon its initially waking up from the sleep mode, the low frequency clock having a lower operating frequency and a lower power consumption than the high frequency clock, the CPU operating at the clock rate of the low frequency clock upon initially being awakened from the sleep mode.

23. The method according to claim 22, further including:

performing a check of pending operations at the low clock frequency to determine the number of operations which are pending upon being awakened from the sleep mode;

maintaining operation of the second clock if the number of operations is below a selected number; and

turning on the high frequency clock and beginning operation of the CPU at the high frequency clock rate in the event the number of pending operations is higher than a predetermined number.

24. The method according to claim 23, further including:

returning to sleep mode after completing the pending operations if the CPU continues to be clocked at the low frequency clock rate indicating that there are a very low number of pending operations and that the CPU is able to return to sleep mode very soon and spending the entire awake cycle being driven by the low frequency clock without the high frequency clock being enabled.

25. The method according to claim 22, further including maintaining operation of a wakeup clock while the CPU is in sleep mode.